ABSTRACT

According to the present invention, a memory circuit requiring refresh operations a first circuit which receives a command in synchronization with a clock signal, and which generates a first internal command internally and a second circuit which generates a second internal command, i.g. a refresh command, internally in a prescribed refresh cycle. And an internal circuit, according to said first internal command, executes corresponding control through clock-synchronous operations, and when said refresh command is issued, sequentially executes control corresponding to the refresh command and control corresponding to said first internal command through clock-asynchronous operations. According to the present invention, when a refresh timing signal is generated, the refresh operation can be intrupted among the external command operations.